COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims. In particular, claims having the status of "currently amended" are being amended in this preliminary amendment. Claims listed as "canceled" should be deleted from the application before calculating fees.

Claims 1-11 (Canceled)

12. (Original) A Flash memory comprising:

memory elements having respective physical addresses that correspond to logical addresses of the Flash memory;

spare memory elements having respective physical address that do not correspond to the logical addresses of the Flash memory;

a content addressable memory array coupled to receive a logical address signal from an external device for comparison with defect addresses stored in the content addressable memory array;

a memory array having word lines coupled to respective match lines of the content addressable memory array, wherein in response to activation of one of the match lines, the memory array outputs a substitute address signal representing a substitute address stored in a row corresponding to the activated match line; and

multiplexing circuitry connected to select between the logical address signal and the substitute address signal as a physical address signal, the multiplexing circuitry providing the physical address signal for selection of a memory cell being accessed.

13. (Original) The memory of claim 12, wherein each memory element and each spare memory element is a block of memory cells that are connected to permit simultaneous erasure of all of the memory cells in the block.

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SAN JOSE, CA 95120

PH: (408) 927-6700
FX (408) 927-6701

14. (Original) The memory of claim 13, further comprising:

a write data path; and

a read data path, wherein

the blocks are organized into a plurality of array planes, the array planes being connected to the write and read data path so as to permit any one of the array planes to conduct a read operation while any other of the array planes conducts a write operation.

15. (Original) The memory of claim 14, wherein each array plane contains erase circuit that permits the array plane to erase a block in the array plane, while other array planes conduct read and write operations.

16. (Original) The memory of claim 14, wherein each array plane comprises at least one of the spare memory elements.

17. (Original) The memory of claim 16, wherein each array plane comprises a spare global bit line that connects to all blocks in the array plane.

18. (Original) An operating method for a Flash memory, comprising:

storing defect addresses in a content addressable memory array in the Flash memory;

storing substitute addresses in a memory array in the Flash memory;

applying a first logical address from an external device to the content addressable memory array for a comparison operation;

outputting from the memory array a substitute address corresponding to a match line activated as a result of the comparison operation; and

accessing a memory element corresponding to the substitute address instead of a memory element corresponding to the first logical address.

19. (Original) The method of claim 18, further comprising applying a second logical address from the external device directly to a decoder in the Flash memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell.

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20. (Original) The method of claim 19, wherein the first logical address is a block address and the second logical address identifies a memory cell within a block.

21. (Original) The method of claim 20, wherein the second logical address is a row

address.

22. (Original) The method of claim 18, wherein accessing the memory element comprises accessing a first array plane in the Flash memory while a second array plane in the Flash memory conducts a second operation.

23. (Original) The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises writing to a memory cell in the second array plane.

24. (Original) The method of claim 22, wherein accessing the first array plane comprises reading a memory cell in the first array plane, and the second operation comprises erasing a block in the second array plane.

Claims 25-26 (Canceled)

REMARKS

This is a preliminary amendment of the attached patent application, which is a divisional of U.S. Pat. App. No. 09/927,693. This preliminary amendment cancels claims directed to subject matter elected in the parent application.

Applicant requests entry of the amendment before calculation of the fees for filing of the attached patent application.

Please contact the undersigned attorney at (408) 927-6700 if there are any questions concerning the application or this preliminary amendment.

EXPRESS MAIL LABEL NO:

EV 232 762 517 US

Respectfully submitted,

David Millers

David Millers
Attorney for Applicant
Reg. No. 37,396

THE PATENT LAW OFFICES
OF DAVID MILLERS

6560 ASHFIELD COURT
SAN JOSE, CA 95120

PH: (408) 927-6700
FX (408) 927-6701